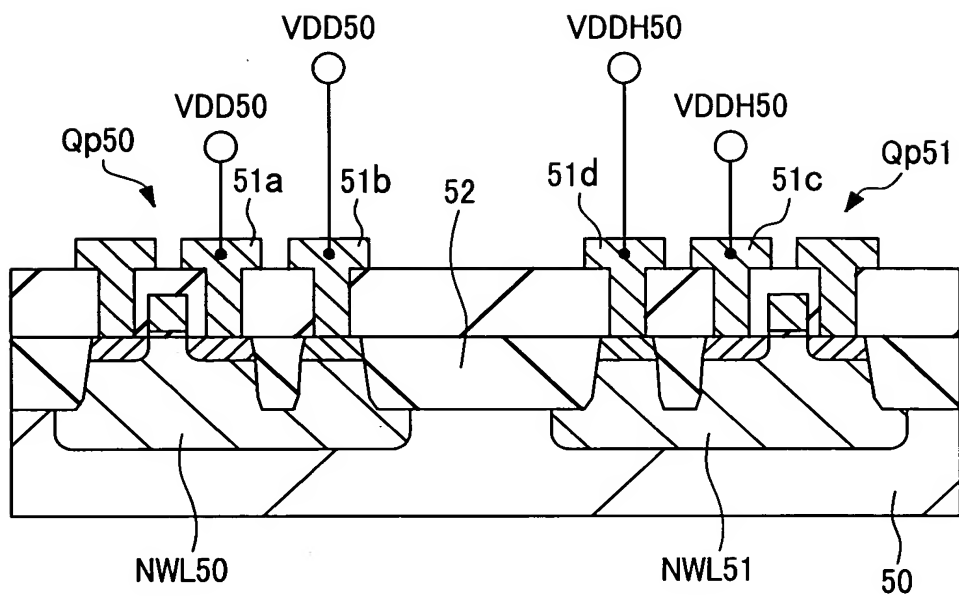
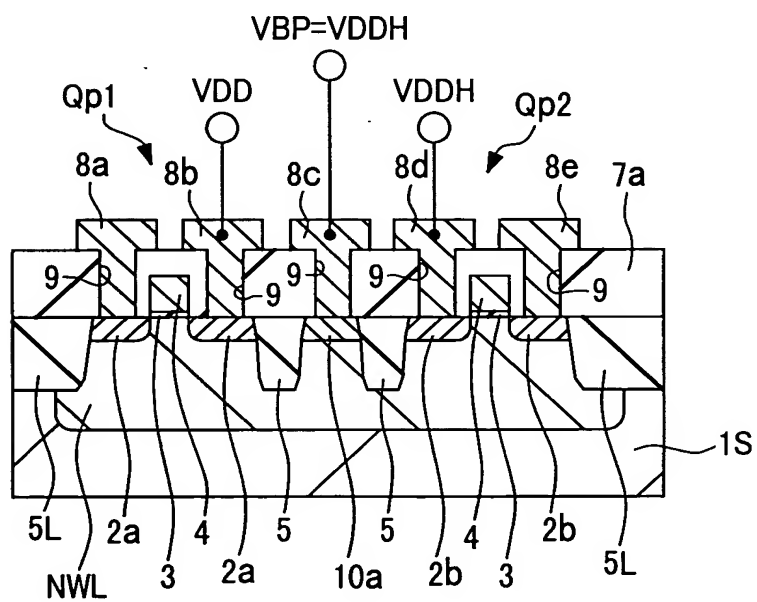


# FIG.1

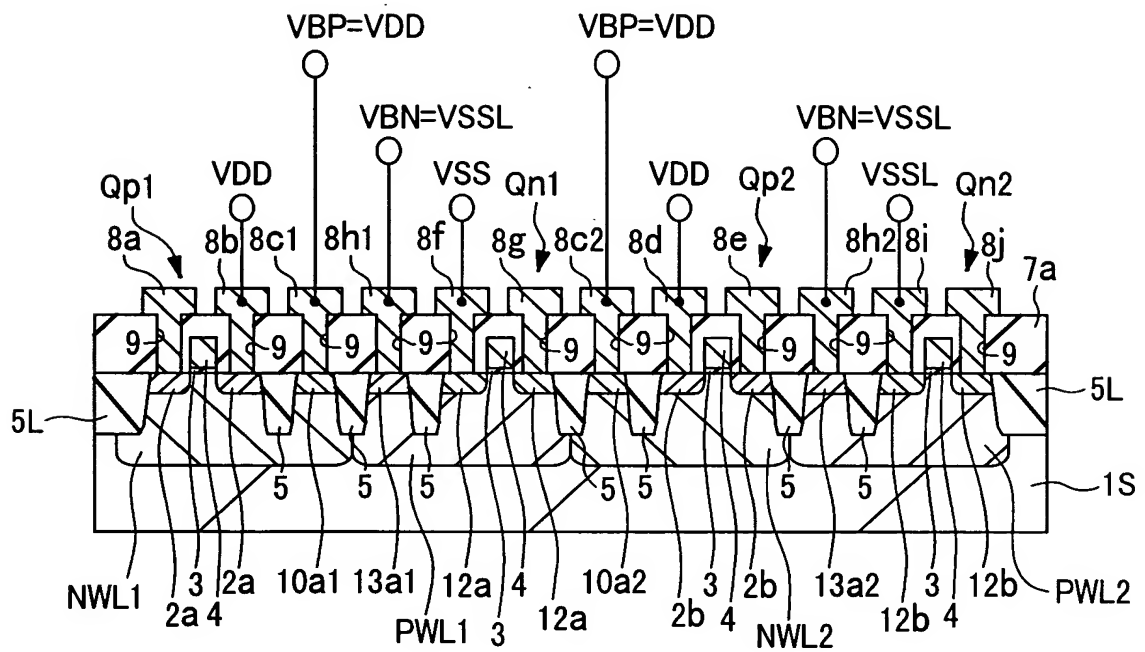


# FIG.2

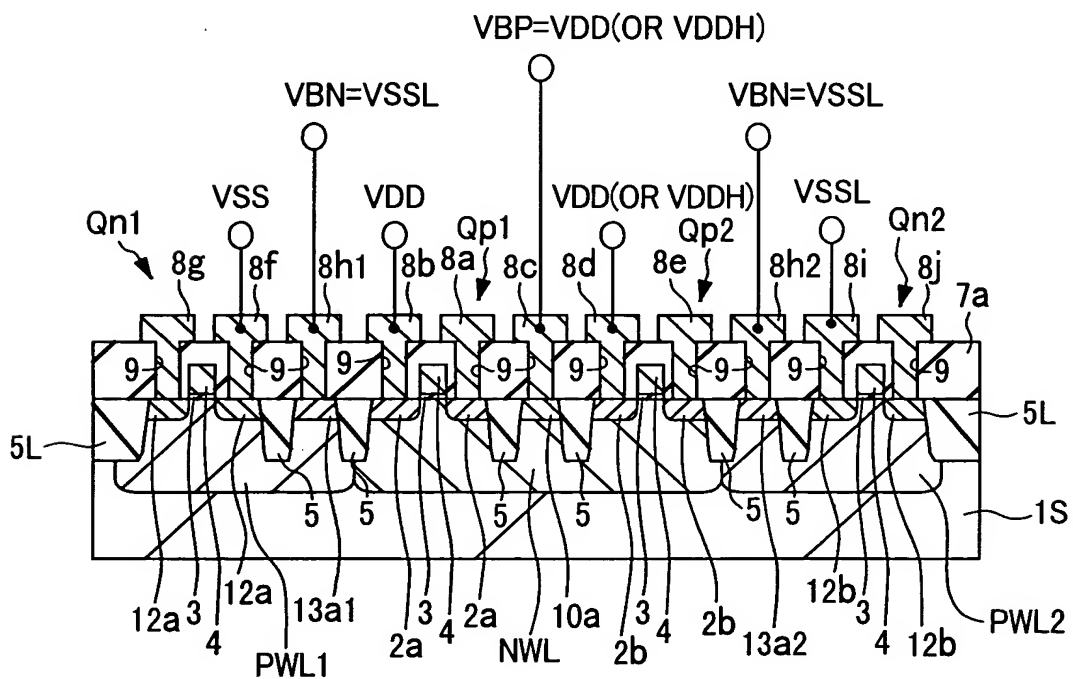


This cross-sectional view illustrates the structure of the semiconductor device. It shows two gate arrays, 50 and 51, separated by a gap 52. Each gate array consists of a substrate with multiple layers: a diffusion layer (DNWL), a nitride layer (NWL), and a polysilicon layer (PWL). The gates are formed by a stack of materials, including a gate oxide (51a, 51b, 51c, 51d, 51e, 51f, 51g, 51h) and a gate stack (51i, 51j, 51k, 51l, 51m, 51n, 51o, 51p). The gates are connected to power supply lines (VDD50, VSS50, VDDH50, VSS50) and signal lines (Qp50, Qn50, Qp51, Qn51). The device is shown in a cross-sectional view, with the layers and gates clearly defined.

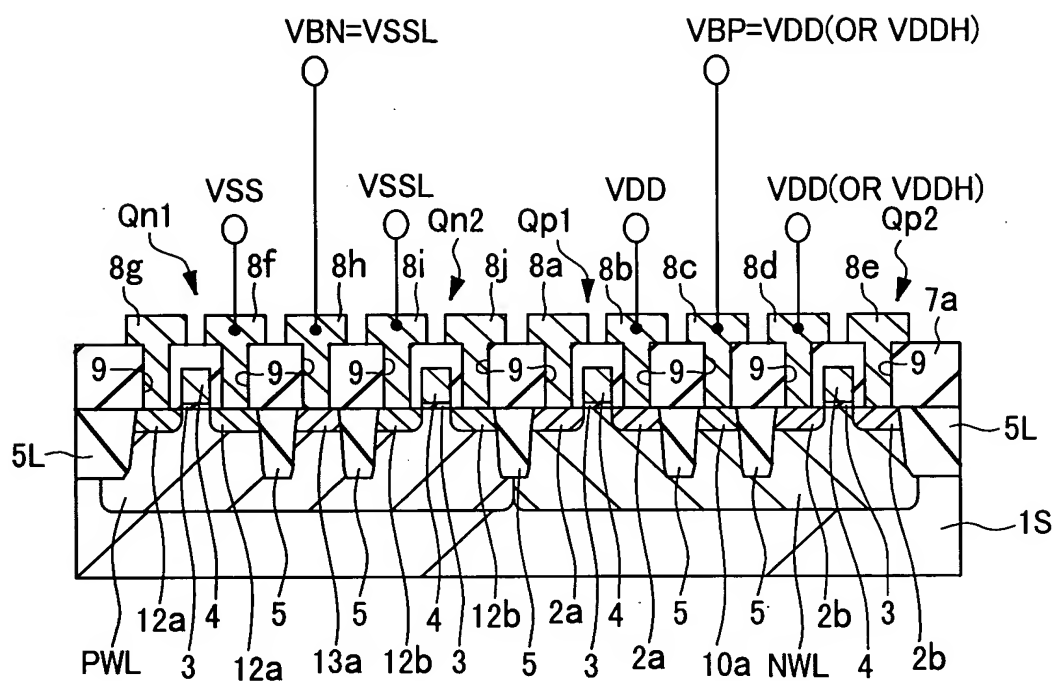
# FIG.5



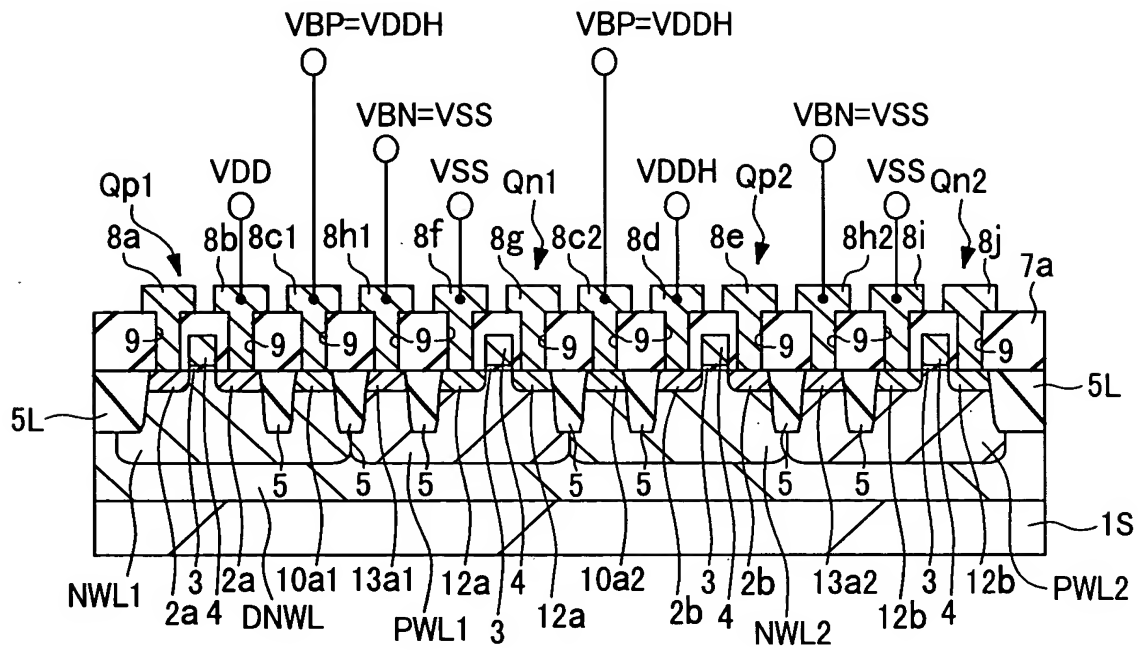
# FIG.6



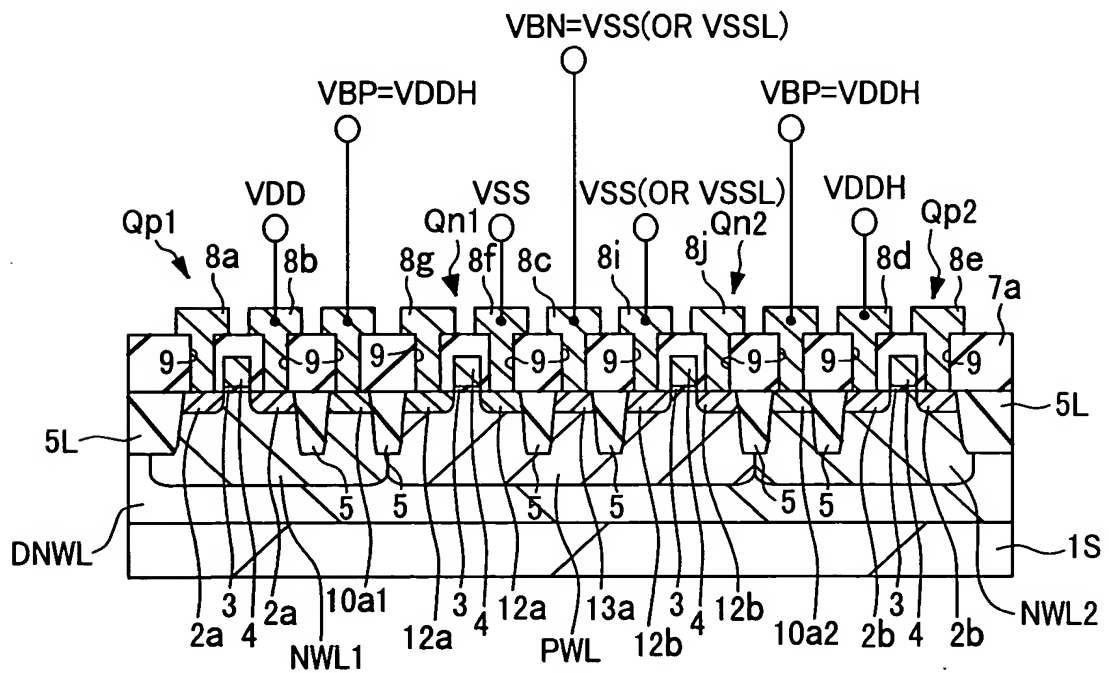
# FIG.7



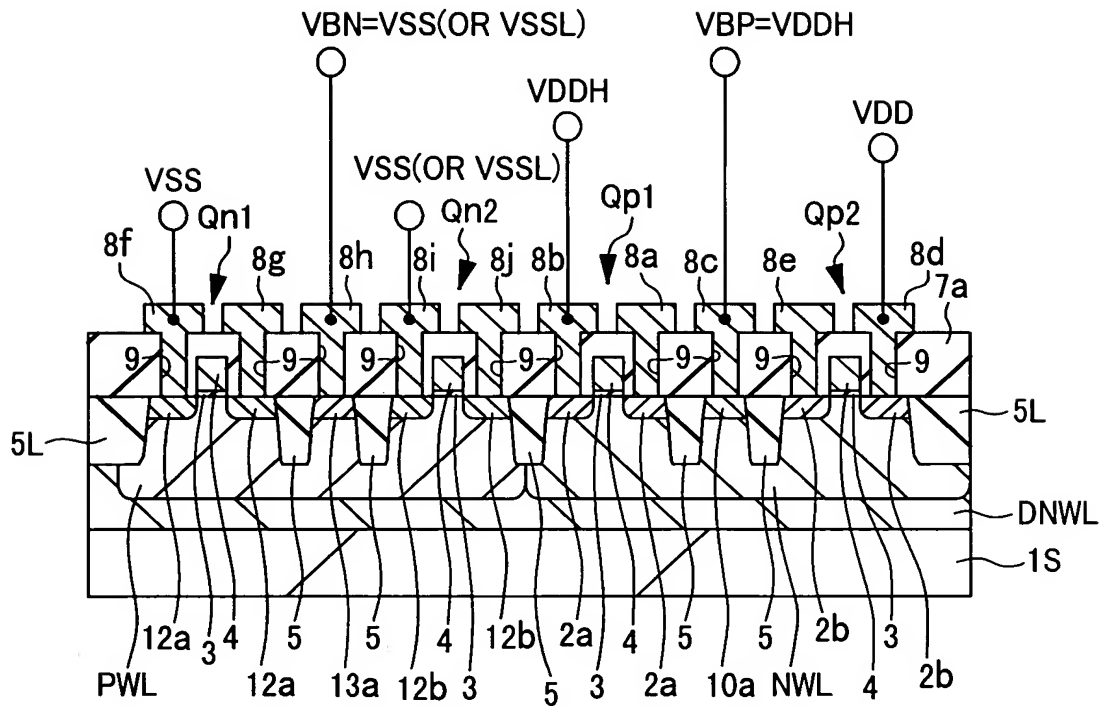
# FIG.8



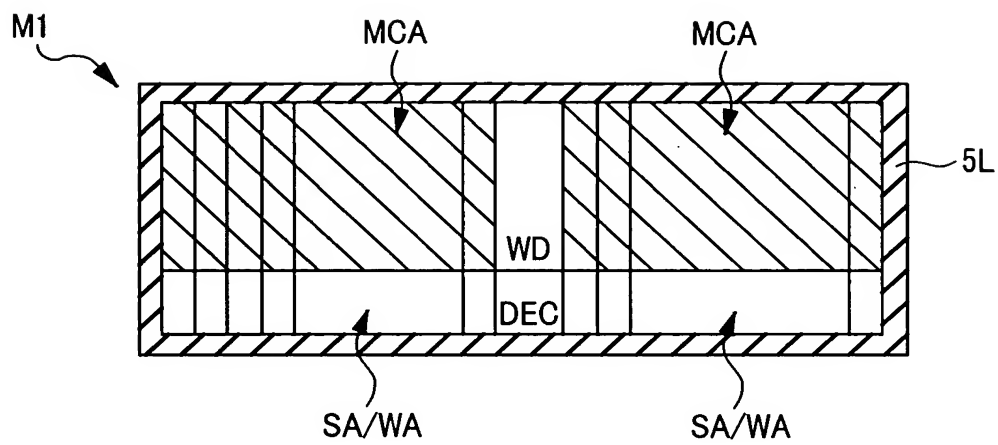
# FIG.9



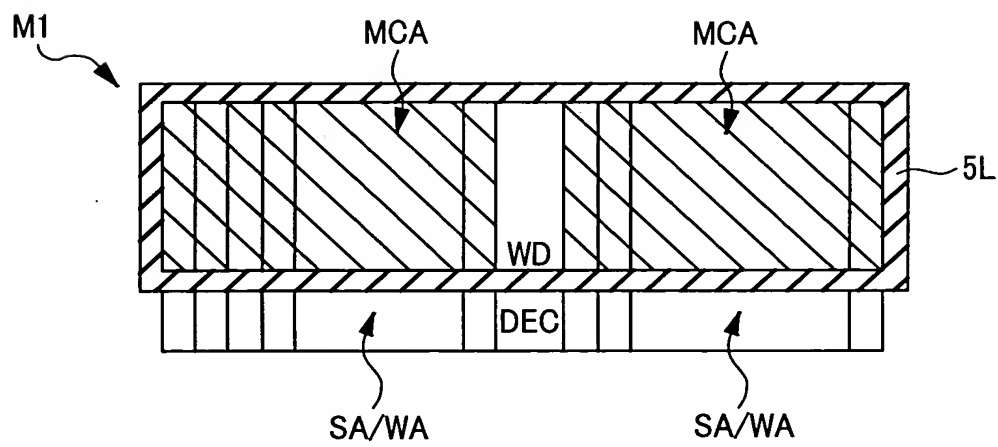
# FIG.10



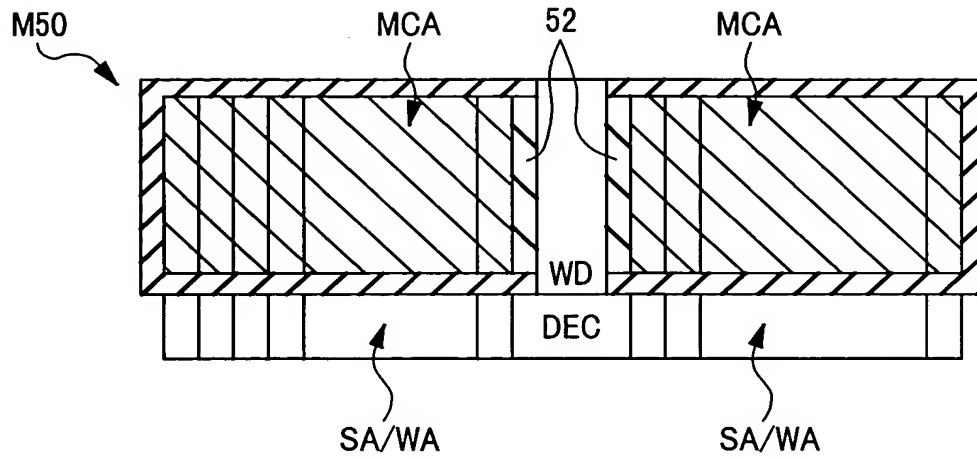
# FIG.11



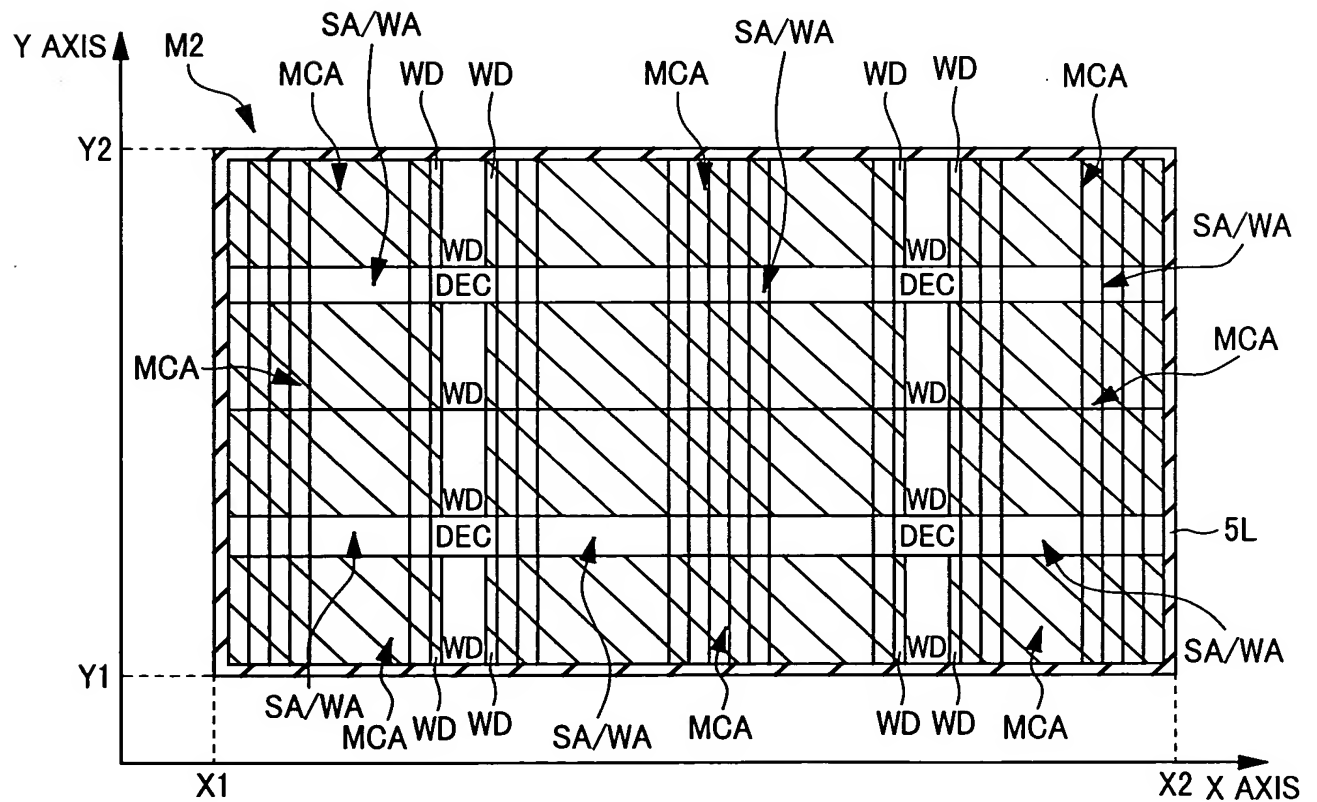
# FIG.12



# FIG.13

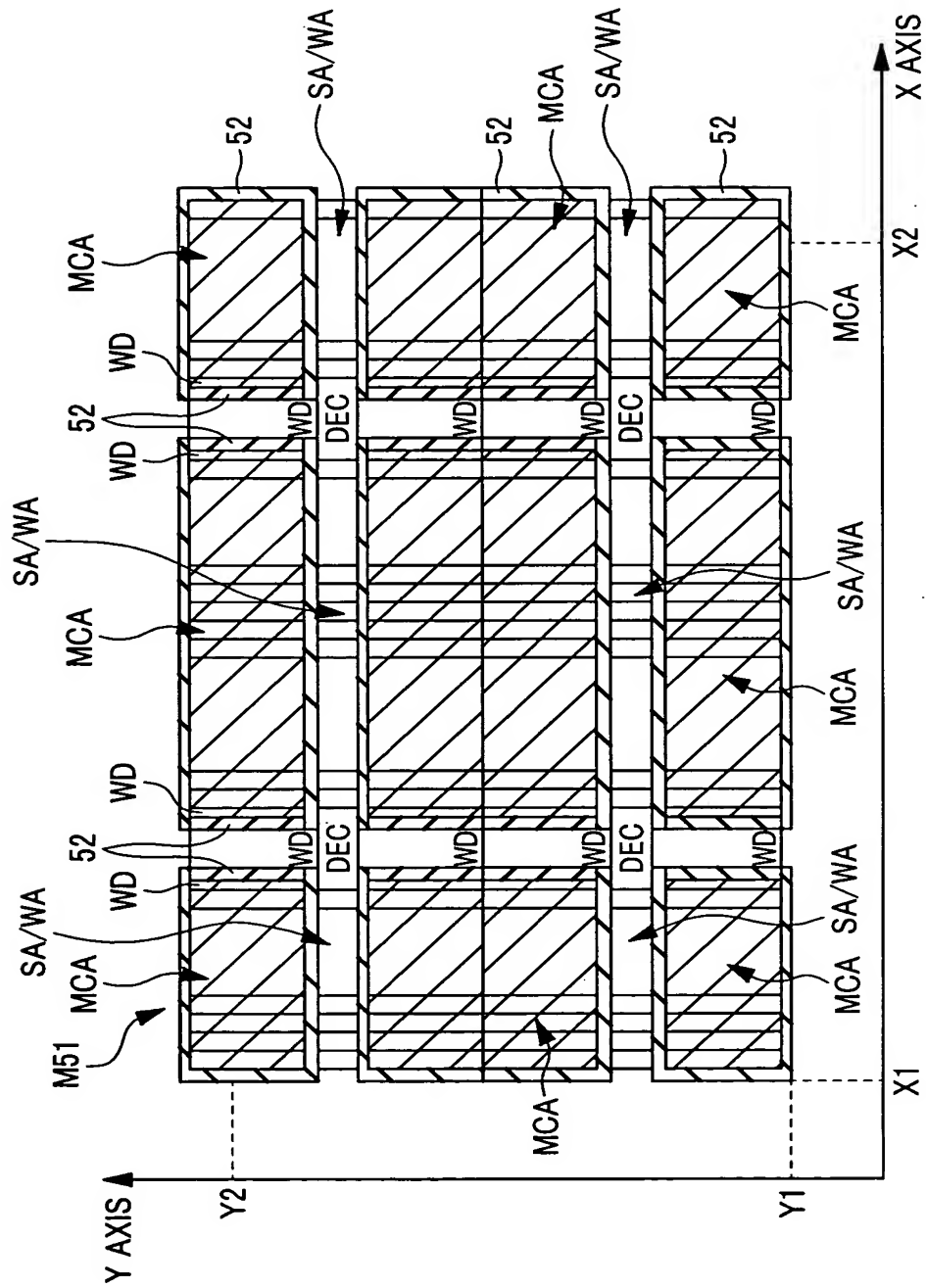


# FIG.14

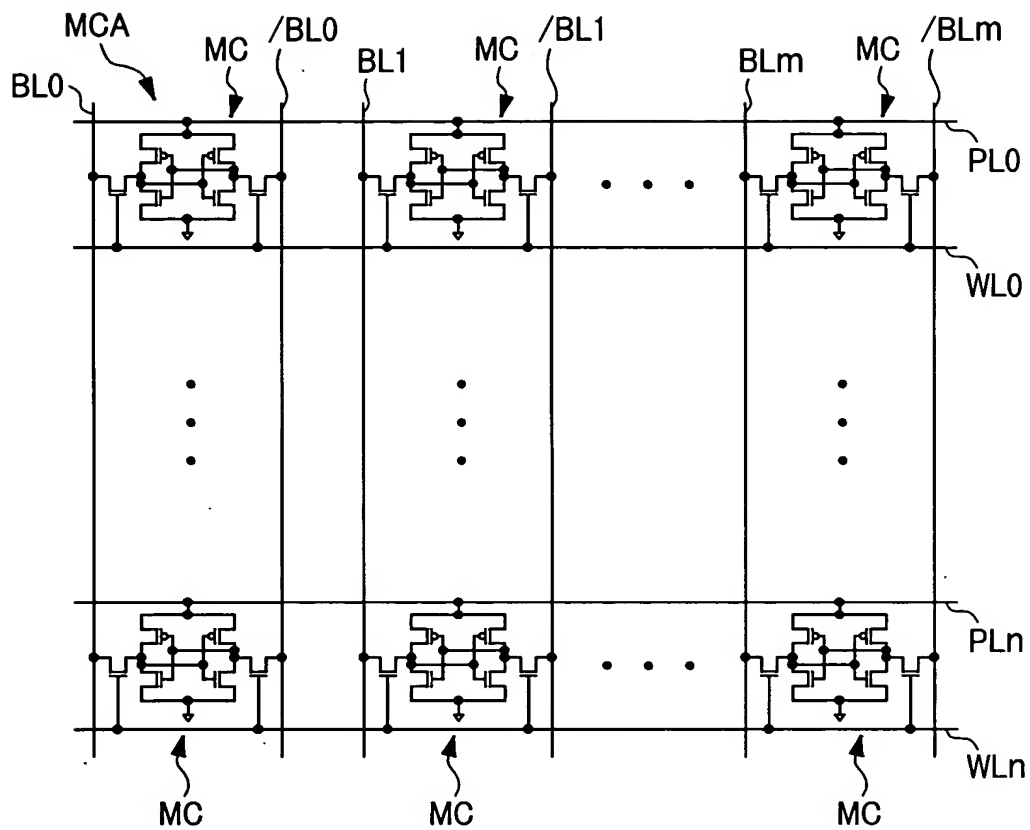




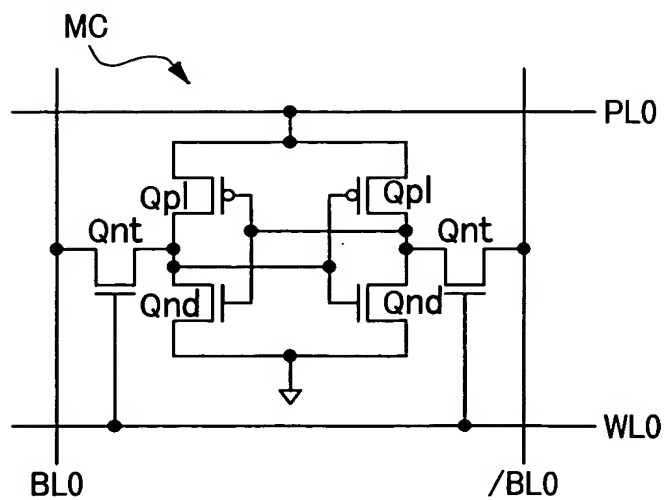
# FIG.15



# FIG.16



# FIG.17



# FIG.18

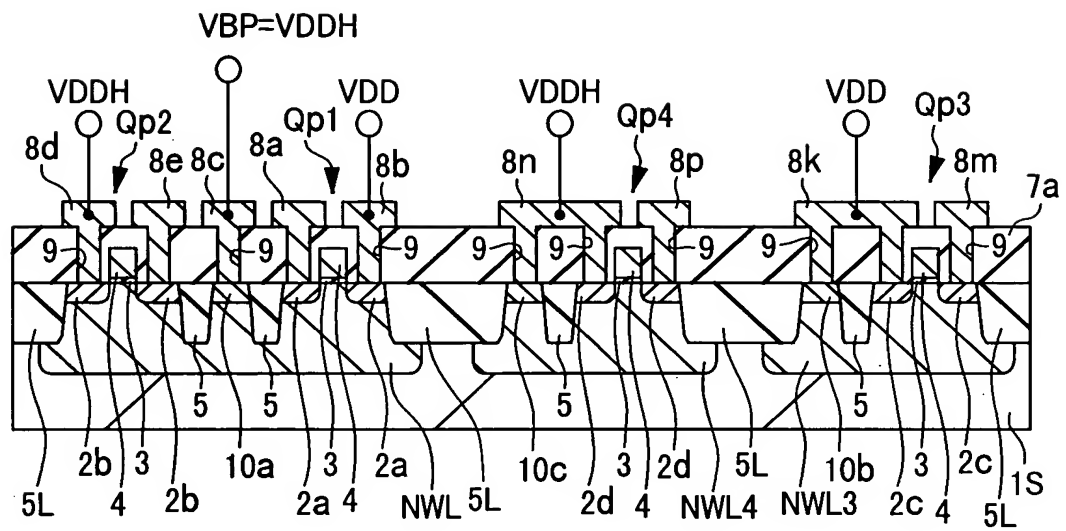
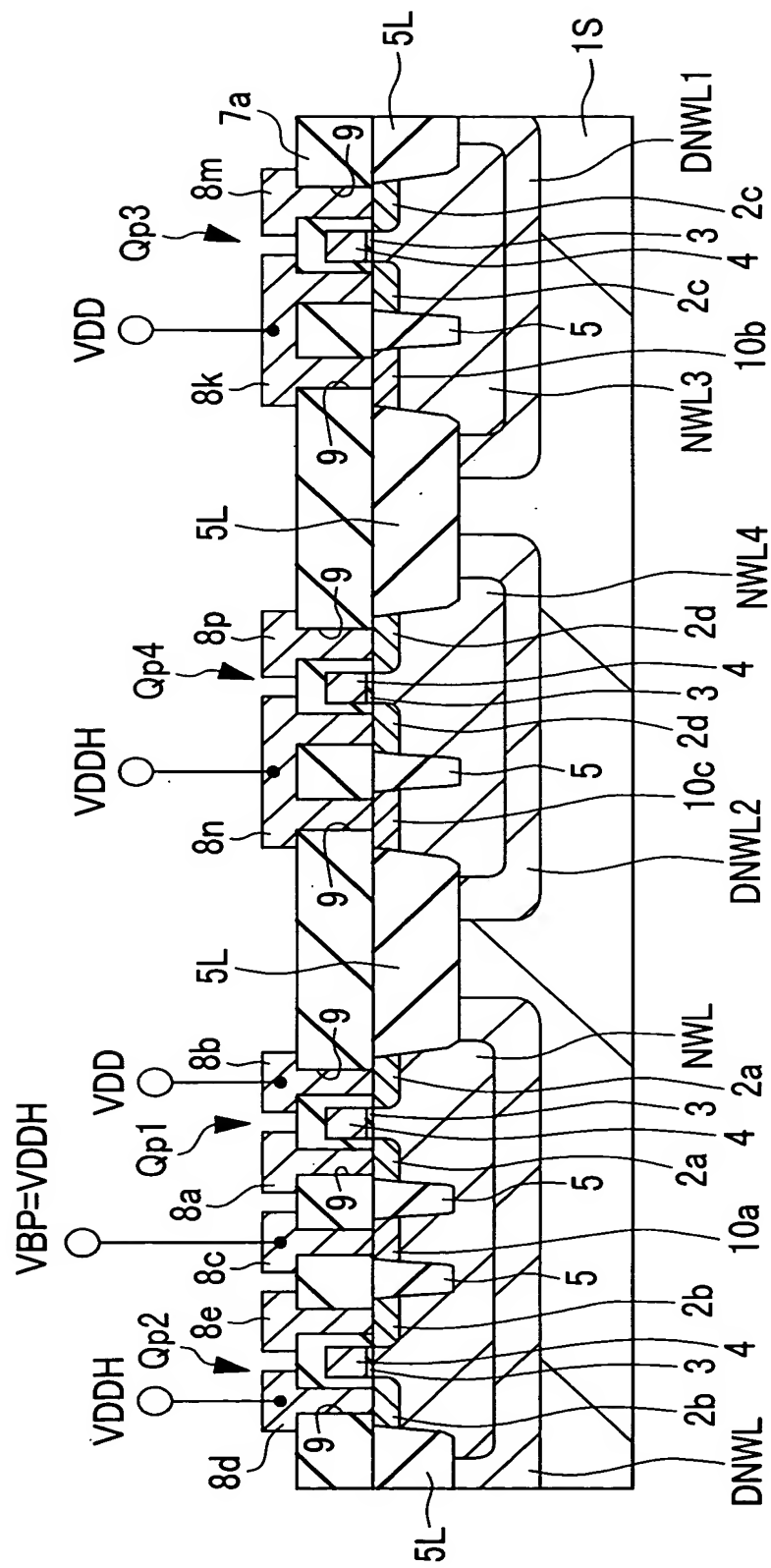


FIG.19



# FIG.20

